AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1-21. (Cancelled)

22. (Previously presented) A method of forming a Schottky barrier diode comprising:

forming a substrate region of a first conductivity type underneath a semiconductor material layer of the same conductivity type;

forming a metal layer; and

forming at least two doped regions of a second conductive type formed in said semiconductor material layer, each one of said doped regions being disposed under said metal layer and being separated from the other doped region and said substrate region by portions of said semiconductor layer, wherein said doped regions are formed by successive implants to form a plurality of stacked bubbles.

23. (Previously presented) The method according to claim 22, further comprising thermally processing said plurality of stacked bubbles.

24. (Previously presented) The method according to claim 22, further comprising implanting said doped regions at a dose between 1×10^{12} and 5×10^{13} per cm^2.

25. (Currently amended) The method according to claim 22, in which the resistivity of said semiconductor material layer is less than five Ohm-cm <u>for a breakdown voltage higher than 200V</u>.

26. (Previously presented) The method according to claim 22, in which said semiconductor material layer comprises a first resistivity value, and said doped regions each comprise a second resistivity value, wherein said second resistivity value is higher than said first resistivity value.

27. (Previously presented) The method according to claim 22, in which said substrate comprises a doping value higher than a doping value of said semiconductor material layer.

28. (Previously presented) The method according to claim 22, in which said doped regions further comprise respective body regions.

29. (Previously presented) The method according to claim 22, in which said doped regions further comprise heavily doped body regions having the same conductivity type of said doped regions.

30. (Previously presented) The method according to claim 22, in which said semiconductor material layer comprises a resistivity value lower than five Ohm-cm for a breakdown voltage higher than 200V.

31. (Previously presented) The method according to claim 22, in which said doped regions comprise P-type doped regions.

32. (Previously presented) The method according to claim 22, in which said semiconductor material layer comprises an N-type semiconductor material layer.

33. (Previously presented) The method according to claim 22, in which said Schottky barrier diode is operational at a voltage of 500V.

34. (Previously presented) The method according to claim 22, in which said Schottky barrier diode is operational at a voltage of 600V.

35. (Previously presented) The method according to claim 22 further comprising a silicide layer formed over the surface of the semiconductor material layer.

36. (Previously presented) The method according to claim 22 in which at least one of the doped regions is in an active area of said Schottky barrier diode and at least one of the doped regions is in an edge area of said Schottky barrier diode.

37. (Previously presented) The method according to claim 22, in which said doped regions are formed by successive implants into successive growths of said semiconductor material layer.

38. (Previously presented) The method according to claim 37, further comprising thermally processing said plurality of stacked bubbles.

39. (Previously presented) The method according to claim 37, further comprising implanting said doped regions at a dose between 1×10^{12} and 5×10^{13} per cm^2.

40. (Currently amended) The method according to claim 37, in which the resistivity of said semiconductor material layer is less than five Ohm-cm for a breakdown voltage higher than 200V.